AMENDMENTS TO THE SPECIFICATION

Please amend the Title of the Invention as follows:

DEVICE HAVING IMPROVED ~~METHOD OF IMPROVING~~ SURFACE PLANARITY PRIOR TO MRAM BIT MATERIAL DEPOSITION

Amend the specification as follows:

[0043] Hence, in an exemplary embodiment of the present invention as shown in FIG. 12, a second conductor layer or material layer 63 is formed over the upper surface of barrier layer 59, metal line 62 and insulating layer 54. Consequently, roughened portions 62a and protruding portions 59a are conformally covered by the second conductor layer 63. The second conductor layer 63 may comprise bonding materials such as tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) or chromium (Cr), among others. In a preferred embodiment of the invention, the conductor layer 63 is formed of sputtered tantalum. In this embodiment, tantalum is deposited to a thickness of about 5 nm to about 50 nm. In addition, this layer may be used as a series resistor by including a resistive material such as TaN, ~~WsiN~~ WSiN or other materials. The resistor layer can be deposited under the metal layer to be smoothed in order to preserve its thickness or in place of the conductor layer 63.

[0044] Next, as shown in FIG. 13, second conductor layer 63 is lightly polished to provide a planar surface for the subsequent fabrication of MRAM structures 100 (as described below). The term "lightly polished" is defined herein as polishing enough to planarize or flatten the second conductor layer 63 but not enough to pattern define. In other words, a top portion of the second conductor layer 63 is planarized and a lower portion of the second conductor layer 63 remains intact, conformally covering

roughened portions 62a and protruding portions 59a. The portions of conductor layer 63 overlying insulating layer 54 ~~is~~ are etched in subsequent steps (i.e., defining of the magnetic stack). Note, although roughened portions 62a and protruding portions 59a are not shown, they are still present in the intermediate structure of FIG. 13. However, as noted above, they are covered by the planarized second conductor layer 63 and ~~has~~ have been omitted from FIG. 13 for simplicity. Further, in the proceeding Figures, conductor layer 63 is shown as simply the interface for the MRAM structure 100 and the metal line 62/barrier layer 59.

[0050] In an exemplary embodiment of the present invention, the conductive layer 85 may be formed of tungsten nitrogen (WN), which is deposited to a thickness of about 100-400 Angstroms, more preferably of about 200-300 Angstroms. However, the invention is not limited to this exemplary embodiment[[,]]; this layer may be comprised of a resistive material such as WN, TaN, ~~WsiN~~ WSiN, and others. This layer may act as a series resistor and or a ~~cmp~~ CMP stopping layer dependent on the material and thickness chosen. Materials such as a-c amorphous carbon, various oxides and nitrides may be used as ~~cmp~~ CMP stops as well as series resistors.

[0053] Subsequent to the formation of the insulating layer 95 (FIG. 19), portions of the insulating layer 95 that are formed over the top surface of the MRAM structures 100 are removed by means of chemical mechanical polishing (CMP) or well-known RIE dry etching processes. In an exemplary embodiment of the invention, the insulating layer 95 is chemical mechanical polished so that an abrasive ~~abravise~~ polish removes the top surface of the insulating layer 95 above the MRAM structures 100, down to or near the planar surface of the top surface of the conductive layer 85, to form respective MRAM contacts 99 in a polished insulating layer 96, as illustrated in FIG. 20.

This way, the conductive layer 85, which was formed as part of the sense layer 92 of the MRAM structure 100, acts as a polishing stop layer in the formation of the contacts 99.